REMARKS

Claims 1, 6, 12 and 20 have been amended to more particularly point out applicants' invention. New claims 27-31 have been added. Support for the amendments and the new claims can be found throughout the originally filed specification, for example on pages 15-18 of the originally filed specification, Figure 1, and Figure 3, demonstrating the presence of oxygen and showing analogous depth distribution of oxygen and Ni, as an evidence of formation of nickel oxide. No new matter has been added.

Examiner Douglas Willie is thanked for the courtesy extended to Applicants' representative during a personal interview on February 21, 2001.

Claims 1, 2, 4-11 and 20 are rejected under 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants' regard as their invention. It is believed that the rejection is moot in view of the amendment to claim 1.

Claims 12-14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al. ('422).

Claims 1, 2, 4-11, 20 and 22-26 are rejected under 35 U.S.C. 103(a) as being obvious over Nakamura et al. ('422) in view of Manabe et al. and Nakamura et al. ('350). These rejections are respectfully traversed for at least the following reasons.

Claims 1, 2 and 4-11 are drawn to a semi-conductor device having a Group III nitride compound semiconductor comprising a surface layer made of p-type conduction, an electrode layer formed on said surface layer, and a three-layer electrode pad formed on a portion of an electrode layer. The electrode pad consists of Ni/Au, and Al layer is formed as an upper layer. In the device, portions of the electrode pad are covered with a protective film. The

protective film is formed as follows. First, the electrode pad is covered uniformly by the protective film. A portion of the protective film is etched off. A mask having a window or windows is placed over the protective film and etching solution is applied to the window. When the top layer of the pad is made of gold, due to weak adhesiveness between gold and the protective layer, etching solution permeates into clearance existing at the junction plane of the protective film and the Au layer. As a result, the protective film is etched more than necessary, as it is shown on Figure 5B, compromising the function of the protective film. Applicants have found, that using Al to form the top layer of at least the portions of the electrode pad, where a window is formed eliminated the problem of over-etching due to much stronger adhesive forces between the protective film and Al layer. In short, the electrode pad comprises three layers and only the layer formed on the top of the electrode pad is made of aluminum (A1). The claimed invention, is, therefore not suggested by combined teachings of Nakamura and Manabe.

The invention claimed in claims 12-14 and 22-26 is directed to a semiconductor devise wherein the portion of the material of the second electrode layer which is uncovered by an electrode pad is distributed more deeply into the surface layer than the first layer. The claims specifically require that such reverse distribution is obtained by heat treatment in an atmosphere comprising oxygen. The reverse distribution of layers only occurs in an oxidative atmosphere. Nakamura does not teach or suggest carrying out heat treatment in an atmosphere including oxygen. In fact, Nakamura et al. discloses that "it is preferred that the annealing treatment in the present invention be conducted under a **non-oxidative** or inert atmosphere, such as nitrogen" (col. 6, lines 5-7, emphasis added). In the experimental data submitted by Applicants, the inverse distribution of nickel (Ni) and gold (Au) was examined under three conditions: a heating process with oxygen, illustrated by Figures A-1, A-2L, and

A-2S; a process with no heat treatment, illustrated in Figure 3; and a process in a non-oxidative environment consisting of pure nitrogen, illustrated by Figures A-4 and A-5

Analyzing the inverse distribution in the depth direction as illustrated in Figures A-1, A-2L, and A-2S, nickel (Ni) and gold (Au) are inverted in the presence of heat and oxygen. When the heating process is not carried out, as illustrated in Figure A-3, or when there is no oxygen (as in Nakamura et al.) in the atmosphere, as illustrated in Figures A-4 and A-5, no transfer of nickel (Ni) and gold (Au) is observed. Illustrative Example discussed on pages 15-17 of the originally filed application demonstrates results similar to those in Figures A-1, A-2L and A-2S wherein the heat treatment is conducted in the presence of oxygen. The experimental conditions for the illustrative example are such that residual oxygen remains in the heat treatment atmosphere upon initial evacuation of the chamber to less than 1 m Torr. Upon filling the chamber with nitrogen the atmosphere in the chamber is not inert due to the presence of small quantities of oxygen, sufficient to facilitate the layer inversion. Consequently, the present invention is neither anticipated nor rendered obvious by Nakamura et al.

Furthermore, Nakamura does not teach or suggest that a p-type semiconductor material of the surface layer and metals of the second electrode layer are alloyed, which results in improvement of ohmic characteristic of the device. In particular, Nakamura does not disclose that gold (Au) and a p-type gallium nitride compound semiconductor are alloyed.

Moreover, Nakamura does not disclose that metals of the first electrode layer form oxides. Specifically, Nakamura fails to disclose that the first electrode layer becomes nickel oxide after carrying out heat treatment. These results are demonstrated in the experimental data presented in Figs. A-1, A-2L and A-2S, and original Figure 3, wherein the distribution of nickels (Ni) is similar to that of oxygen (O).

The Examiner states that the median for Ni in figure A-5 is misplaced. However, the medium value designated on the Figures correspond to a depth than divides the amount of metal in equal parts, i.e., 50 % of the total amount of metal is positioned above this depth and 50 % of the total amount of metal is positioned below this depth. Therefore, the medium values for Ni and Au as shown on all the Figures, including Figure A-5 are correct.

Applicants respectfully submit that the application is now in condition for allowance, and a Notice to that effect is earnestly solicited.

Respectfully submitted,

PILLSBURY WINTHROP, LLP

By: ______________________

Dale S. Lazar
Reg. No. 28,872
Tel. (202) 861-3527

DSL/ISZ
1100 New York Avenue, N.W.
Ninth Floor
Washington, D.C. 20005-3918
(202) 861-3000

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Four Times Amended) A [lighting-emitting] light-emitting semiconductor device having a Group III nitride compound semiconductor comprising:

a surface layer made of [with] p-type conduction;

an electrode layer formed on said surface layer; and

an electrode pad comprising:

a first metal layer formed on [an] said electrode layer formed on said surface layer, a second metal layer formed on said first metal layer, and a third metal layer formed on said second metal layer; and

a protective film over said third metal layer, said protective film leaving exposed a central portion of said third metal layer; said electrode layer being capable of passing an emitted light;

said electrode pad being capable of supplying a current to said electrode layer; and

wherein said second metal layer is made of gold (Au), said first metal layer comprises a material that has an ionization potential lower than gold (Au), and said third metal layer comprises aluminum (Al) that has an adhesiveness to said protection film which is stronger than gold (Au)[, said second metal layer being distributed more deeply into said semiconductor than that of said first metal layer by heat treatment].

6. (Twice Amended) The light-emitting semiconductor device according to claim 1, wherein said electrode layer has a multi-layer structure having at least a first electrode layer

formed on said [semiconductor] surface layer and a second electrode layer formed on said first electrode layer, wherein said first electrode layer comprises material having an ionization potential that is lower than that of said second electrode layer, said material of said second electrode layer, has an ohmic characteristic to said [semiconductor] surface layer better than that of said first electrode layer, and said material of said second electrode layer being distributed more deeply into said [semiconductor] surface layer than that of said first electrode layer by heat treatment.

12. (Twice Amended) A light-emitting semiconductor device having a Group III nitride compound semiconductor comprising:

a surface layer [with] made of p-type [conduction] semiconductor;

a multi-layered electrode layer comprising a first electrode layer formed on said surface layer and a second electrode layer formed on said first electrode layer;

an electrode pad covering a portion of said second electrode layer and leaving another portion of said second electrode layer uncovered; and

wherein said first electrode layer comprises a material which has an ionization potential lower than that of said second electrode layer,

said second electrode layer comprises a material which has an ohmic characteristic to said semiconductor better than that of said first electrode layer, and

the portion of said material of said second electrode layer which is uncovered by said electrode pad is distributed more deeply into said surface layer than that of said first electrode layer by heat treatment in atmosphere comprising oxygen and provides a contact resistance between said electrode layer and said surface layer lower than said portion covered with said electrode pad.

20. (Twice Amended) The light-emitting semiconductor device according to claim 6, wherein materials of said second electrode layer do not permeate into said first electrode layer directly under said electrode pad, which enables the interface between said electrode layer and said [semiconductor] <u>surface layer</u> directly under said electrode pad to have a large resistivity and not have electric current pass therethrough.

Claims 27-31 have been added as new claims.